Amendments to the Specification:

Please replace paragraph [0018] with the following amended paragraph:

[0018] More detail is now provided with respect to the structures forming synthesizer 100 and the operation of those structures. When the phase output signal, Φ_{out} , is leading the phase reference signal, Φ_{ref}, phase detector 105 generates a ~~an~~ DOWN signal with a logic high at its DOWN output. Conversely, when the phase output signal, Φ_{out} , is lagging the phase reference signal, Φ_{ref}, detector 105 generates an UP signal with a logic high at its UP output. The phase detector UP output is connected to input 205A of direct path charge pump 200 as shown. The phase detector DOWN output is connected to input 205B of direct path charge pump 200 as shown. When the UP signal exhibits a logic high, the DOWN signal exhibits a logic low, and vice versa.

Please replace paragraph [0028] with the following amended paragraph:

[0028] An amplifier 800 is used to combine the outputs of the direct and integrating paths and to provide a high-pole filter to further attenuate any high frequency energies which might otherwise reach VCO 805. More specifically, the inverting input of amplifier 800 is coupled by via switch 810 and capacitor 815 to filter outputs 600B and 700B. A switch 820 is coupled between ground and the junction of capacitor 815 and switch 810 to enable discharge of capacitor 815 to ground under the control of the reset signal, RST. Switch 810 enables sampling of the loop filter signals from capacitor 815 under the control of sampling signal, SMP. A capacitor 825 is coupled between the inverting input of amplifier 800 and the output of amplifier 800. The non-inverting input of amplifier 800 is coupled to ground. The output of amplifier 800 is coupled to the input of VCO 805 to instruct VCO 805 regarding the phase of the output signal Φ_{out} which the VCO should generate by phase lock loop action.